1. A branch apparatus within a microprocessor that utilizes a fetch address to select a cache line in an instruction cache, the apparatus also using the fetch address to speculatively predict whether a branch instruction will be taken or not taken, the branch instruction potentially being present in the instruction cache line, the apparatus comprising:

a first predictor, coupled to the fetch address, for predicting whether the branch instruction will be taken or not taken based on the fetch address;

logic, coupled to the fetch address, for providing a binary function of the fetch address and a global branch history on an output of said logic;

a second predictor, coupled to said logic output, for predicting whether the branch instruction will be taken or not taken based on said output; and

a selector, coupled to the fetch address, for selecting one of said first and second predictors based on the fetch address.

2. The apparatus of claim 1, wherein said binary function comprises an exclusive OR of at least a portion of the fetch address and said global branch history.

3. The apparatus of claim 1, wherein said first predictor is provided by a branch target address cache indexed by the fetch address.

4. The apparatus of claim 1, wherein said second predictor is provided by a branch history table indexed by said binary function of the fetch address and said global branch history.

5. The apparatus of claim 1, wherein said selector is provided by a branch target address cache indexed by the fetch address.

6. The apparatus of claim 1, wherein said selector comprises a bit for selecting between said first and second predictions.

7. The apparatus of claim 1, wherein each of said first and second predictors comprises a plurality of predictors of whether the branch instruction will be taken or not taken, wherein said selector comprises a plurality of bits corresponding to said plurality of predictors, for selecting between corresponding ones of said plurality of first and second predictors.

8. The apparatus of claim 1, wherein said selector comprises a saturating up/down counter.

9. The apparatus of claim 8, wherein said saturating up/down counter stores a selection value from among one of: strongly first predictor, weakly first predictor, weakly second predictor, and strongly second predictor.

10. The apparatus of claim 1, further comprising:

a register, coupled to said second predictor, for storing said global branch history.

11. The apparatus of claim 10, wherein said register comprises an N-bit shift register for storing N previous outcomes of whether branch instructions executed by the microprocessor where taken or not taken.

12. A speculative branch prediction apparatus in a pipelined microprocessor having an instruction cache, the instruction cache receiving a fetch address on an address bus for selecting a cache line in the instruction cache, a branch instruction presumably present in the cache line, the apparatus comprising:

a speculative branch history table (BHT), for providing a first direction prediction of the branch instruction;

a speculative branch target address cache (BTAC), coupled to the address bus, for providing a second direction prediction of the branch instruction, and for providing a selection prediction for selecting between said first and second direction predictions; and

a multiplexer, coupled to said BHT and said BTAC, for selecting one of said first and second direction predictions based on said selection prediction;

wherein said second prediction is provided in response to the fetch address even though the branch instruction may not be present in the instruction cache line.

13. The apparatus of claim 12, further comprising:

a global branch history register, coupled to said BHT, for storing a global history of directions of branch instructions previously executed by the microprocessor.

14. The apparatus of claim 13, wherein said BHT provides said first direction prediction in response to a function of the instruction cache fetch address and said global history stored in said global branch history register.

15. The apparatus of claim 14, wherein said function comprises a logical exclusive OR of said global history stored in said global branch history register and a portion of the instruction cache fetch address.

16. The apparatus of claim 14, wherein said BHT comprises an array of storage elements for storing a plurality of direction predictions, wherein said array is indexed by said function of the instruction cache fetch address and said global history.

17. The apparatus of claim 16, wherein each of said storage elements is configured to store a plurality of

direction predictions for selection as said first direction prediction.

18. The apparatus of claim 12, wherein each of said first direction prediction, said second direction prediction, and said selection prediction comprises a plurality of predictions.

19. The apparatus of claim 18, wherein said multiplexer selects one of said plurality of predictions for each of said first and second direction predictions in response to a corresponding one of said plurality of selection predictions.

20. The apparatus of claim 19, further comprising:

control logic, coupled to said multiplexer, for receiving said one of said plurality of predictions for each of said first and second direction predictions from said multiplexer, said control logic configured to cause the microprocessor to selectively speculatively branch or not branch based on said one of said plurality of predictions.

21. The apparatus of claim 20, wherein said control logic is configured to cause the microprocessor to

selectively speculatively branch to a speculative branch target address provided by said BTAC in response to the fetch address.

22. A speculative branch target address cache (BTAC) in a microprocessor, the BTAC comprising:

an array, configured to store branch instruction direction predictions;

an input, coupled to said array, configured to receive an instruction cache fetch address, said fetch address indexing into said array to select one of said direction predictions; and

an output, coupled to said array, for providing said one of said direction predictions to branch control logic;

wherein the branch control logic causes the microprocessor to speculatively branch if said one of said direction predictions specifies a taken direction, regardless of whether a branch instruction is present in a line of the instruction cache indexed by said fetch address.

23. A microprocessor for speculatively branching, comprising:

an instruction cache, for providing a line of instruction bytes selected by said fetch address provided on an address bus;

a speculative branch history table (BHT), coupled to said address bus, for providing a first prediction of whether a branch instruction that is presumed to be present in said instruction cache line will be taken, said first prediction provided based on a combination of said fetch address and a global branch history;

a speculative branch target address cache (BTAC), coupled to said address bus, for providing a second prediction of said presumed branch instruction and for providing a selector; and

control logic, coupled to said BHT and BTAC, for causing the microprocessor to speculatively branch if one of said first and second predictions selected by said selector predicts that said presumed branch instruction will be taken.

24. The microprocessor of claim 23, wherein said control logic causes the microprocessor to speculatively branch to a speculative branch target address provided by said BTAC based on said fetch address.

25. The microprocessor of claim 23, further comprising:

a speculative call/return stack, coupled to said BTAC, for storing a plurality of speculative return addresses;

wherein said control logic causes the microprocessor to speculatively branch to one of said plurality of speculative return addresses provided by said speculative call/return stack based on said fetch address.

26. The microprocessor of claim 25, wherein said BTAC is configured to provide an indication of whether said presumed branch instruction is a return instruction.

27. The microprocessor of claim 26, wherein said control logic causes the microprocessor to speculatively branch to said one of said plurality of speculative return addresses only if said indication indicates said presumed branch instruction is a return instruction.

28. The microprocessor of claim 27, wherein said BTAC is configured to provide an indication of whether said presumed branch instruction is a call instruction.

29. The microprocessor of claim 28, wherein said control logic causes said one of said plurality of speculative return addresses to be pushed onto said speculative call/return stack if said indication indicates said presumed branch instruction is a call instruction.

30. The microprocessor of claim 23, wherein said selector is updated in response to a resolved direction of whether said presumed branch instruction is taken.

31. The microprocessor of claim 30, wherein said selector is updated in response to said resolved direction if a selected one of said first and second predictions is incorrect, and if a non-selected one of said first and second predictions is correct.

32. The microprocessor of claim 31, wherein said selector is updated by toggling said selector.

33. The microprocessor of claim 31, wherein said selector is updated by counting said selector toward said non-selected prediction.

34. The microprocessor of claim 23, wherein said BHT comprises an array of storage elements, for storing a branch history for each of a plurality of branch instructions.

35. The microprocessor of claim 34, wherein said branch history for each of said plurality of branch instructions comprises a taken/not taken bit.

36. The microprocessor of claim 34, wherein said branch history for each of said plurality of branch instructions comprises a saturating up/down counter.

37. A method for speculatively branching in a microprocessor, the method comprising:

generating a plurality of speculative branch direction predictions of an instruction;

selecting one of said plurality of speculative branch direction predictions as a final direction prediction; and

speculatively branching the microprocessor if said final direction prediction indicates said instruction will be taken;

wherein said generating, said selecting, and said speculatively branching are preformed prior to decoding said instruction.

38. The method of claim 37, further comprising:

detecting said final direction erroneously indicated said instruction will be taken subsequent to said speculatively branching.

39. The method of claim 38, further comprising:

branching to a correct target address in response to said detecting.

40. A method for speculatively branching in a microprocessor, the method comprising:

generating first and second predictions of whether a branch instruction will be taken or not taken, in response to first and second binary functions of an instruction cache fetch address;

selecting one of said first and second predictions as a final prediction, said selecting performed in response to a third binary function of said fetch address; and

speculatively branching the microprocessor if said final prediction specifies said branch instruction will be taken;

wherein said generating, said selecting, and said speculatively branching are performed whether or not said branch instruction is present in an instruction cache line selected by said fetch address.

41. The method of claim 40, wherein said first and second functions are different.

42. The method of claim 40, wherein said second binary function comprises a binary function of said fetch address and a global branch history.

43. The method of claim 42, wherein said second binary function comprises an exclusive OR of at least a portion of said fetch address and said global branch history.

44. The method of claim 40, wherein said first and third binary functions are the same.

45. The method of claim 44, wherein said first and third binary functions comprise a predetermined number of least significant bits of said fetch address.